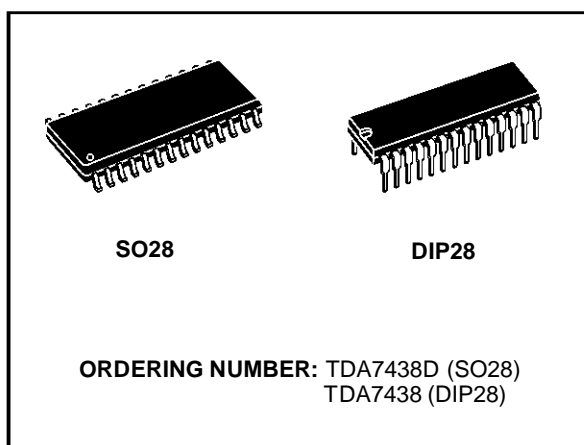


## THREE BANDS DIGITALLY CONTROLLED AUDIO PROCESSOR

PRODUCT PREVIEW

- INPUT MULTIPLEXER
  - 3 STEREO INPUTS
  - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTATION TO DIFFERENT SOURCES
- ONE STEREO OUTPUT
- TREBLE, MIDDLE AND BASS CONTROL IN 2.0dB STEPS
- VOLUME CONTROL IN 1.0dB STEPS
- TWO SPEAKER ATTENUATORS:
  - TWO INDEPENDENT SPEAKER CONTROL IN 1.0dB STEPS FOR BALANCE FACILITY
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTION ARE PROGRAMMABLE VIA SERIAL BUS



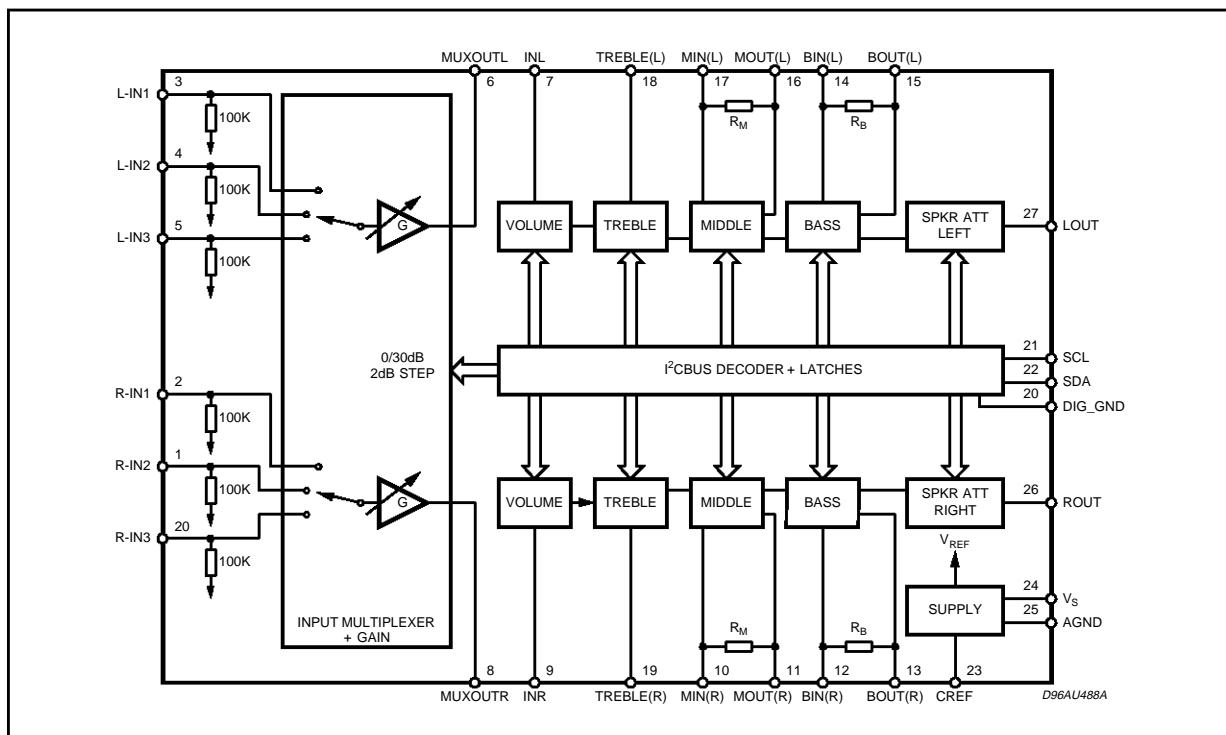
### DESCRIPTION

The TDA7438 is a volume tone (bass, middle and treble) balance (Left/Right) processor for quality audio applications in car-radio and Hi-Fi systems. Selectable input gain is provided. Control of all the functions is accomplished by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

### BLOCK DIAGRAM

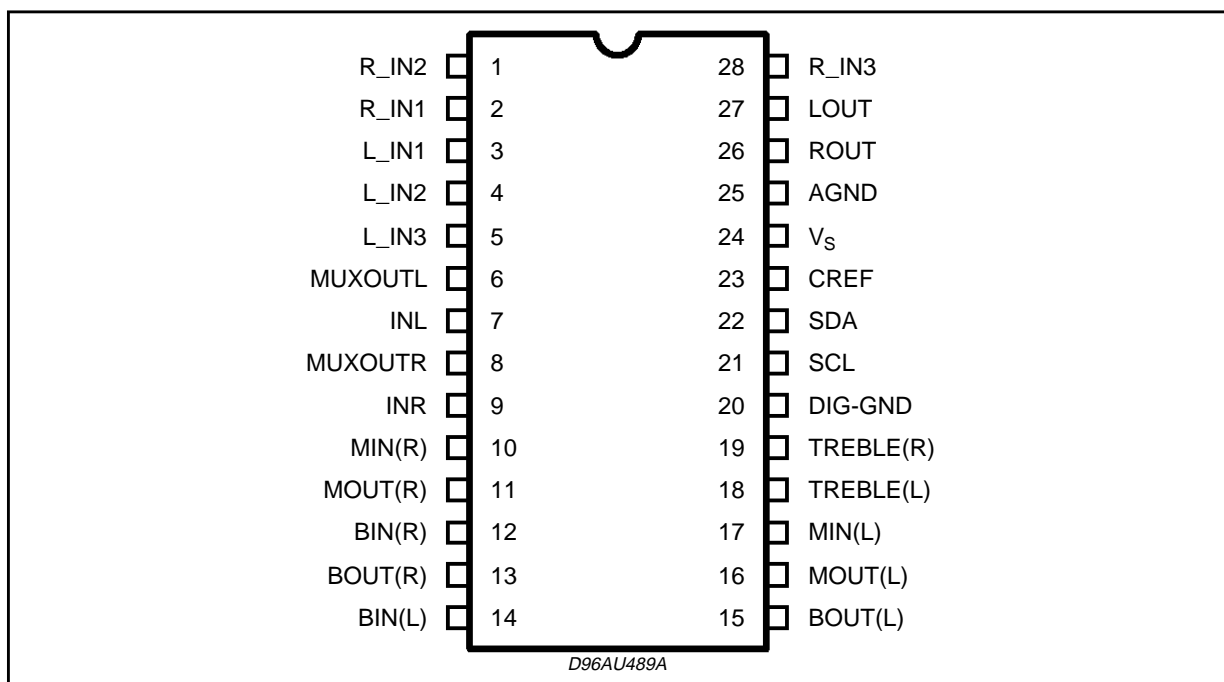


## TDA7438

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_S$	Operating Supply Voltage	11	V
$T_{amb}$	Operating Ambient Temperature	-10 to 85	°C
$T_{stg}$	Storage Temperature Range	-55 to 150	°C

### PIN CONNECTION



### THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-pin}$	Thermal Resistance Junction-pins	85	°C/W

### QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_S$	Supply Voltage	6	9	10.2	V
$V_{CL}$	Max. input signal handling	2			V <sub>rms</sub>
THD	Total Harmonic Distortion $V = 1V_{rms}$ $f = 1KHz$		0.01	0.1	%
S/N	Signal to Noise Ratio $V_{out} = 1V_{rms}$ (mode = OFF)		106		dB
$S_C$	Channel Separation $f = 1KHz$		90		dB
	Input Gain in (2dB step)	0		30	dB
	Volume Control (1dB step)	-47		0	dB
	Treble Control (2dB step)	-14		+14	dB
	Middle Control (2dB step)	-14		+14	dB
	Bass Control (2dB step)	-14		+14	dB
	Balance Control 1dB step	-79		0	dB
	Mute Attenuation		100		dB

**ELECTRICAL CHARACTERISTICS** (refer to the test circuit  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_S = 9\text{V}$ ,  $R_L = 10\text{K}\Omega$ ,  $R_G = 600\Omega$ , all controls flat ( $G = 0\text{dB}$ ), unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>SUPPLY</b>						
$V_S$	Supply Voltage		6	9	10.2	V
$I_S$	Supply Current			7		mA
SVR	Ripple Rejection		60	90		dB
<b>INPUT STAGE</b>						
$R_{IN}$	Input Resistance			100		$\text{K}\Omega$
$V_{CL}$	Clipping Level	THD = 0.3%	2	2.5		V <sub>rms</sub>
$S_{IN}$	Input Separation	The selected input is grounded through a 2.2 $\mu$ capacitor	80	100		dB
$G_{inmin}$	Minimum Input Gain		-1	0	1	dB
$G_{inmax}$	Maximum Input Gain			30		dB
$G_{step}$	Step Resolution			2		dB
<b>VOLUME CONTROL</b>						
$R_i$	Input Resistance		20	33	50	$\text{K}\Omega$
$C_{RANGE}$	Control Range		45	47	49	dB
$A_{VMAX}$	Max. Attenuation		45	47	49	dB
$A_{STEP}$	Step Resolution		0.5	1	1.5	dB
$E_A$	Attenuation Set Error	$A_V = 0$ to $-24\text{dB}$	-1.0	0	1.0	dB
		$A_V = -24$ to $-47\text{dB}$	-1.5	0	1.5	dB
$E_T$	Tracking Error	$A_V = 0$ to $-24\text{dB}$		0	1	dB
		$A_V = -24$ to $-47\text{dB}$		0	2	dB
$V_{DC}$	DC Step	adjacent attenuation steps from 0dB to $A_V$ max		0 0.5	3	mV mV
$A_{mute}$	Mute Attenuation		80	100		dB
<b>BASS CONTROL (1)</b>						
$G_b$	Control Range	Max. Boost/cut	$\pm 12.0$	$\pm 14.0$	$\pm 16.0$	dB
$B_{STEP}$	Step Resolution		1	2	3	dB
$R_B$	Internal Feedback Resistance		33	44	55	$\text{K}\Omega$
<b>TREBLE CONTROL (1)</b>						
$G_t$	Control Range	Max. Boost/cut	$\pm 13.0$	$\pm 14.0$	$\pm 15.0$	dB
$T_{STEP}$	Step Resolution		1	2	3	dB
<b>MIDDLE CONTROL (1)</b>						
$G_m$	Control Range	Max. Boost/cut	$\pm 12.0$	$\pm 14.0$	$\pm 16.0$	dB
$M_{STEP}$	Step Resolution		1	2	3	dB
$R_M$	Internal Feedback Resistance		18.75	25	31.25	$\text{K}\Omega$
<b>SPEAKER ATTENUATORS</b>						
$C_{RANGE}$	Control Range			79		dB
$S_{STEP}$	Step Resolution		0.5	1	1.5	dB
$E_A$	Attenuation Set Error	$A_V = 0$ to $-20\text{dB}$	-1.5	0	1.5	dB
		$A_V = -20$ to $-79\text{dB}$	-3	0	2	dB
$V_{DC}$	DC Step	adjacent attenuation steps		0	3	mV
$A_{mute}$	Mute Attenuation		80	100		dB

## NOTE1:

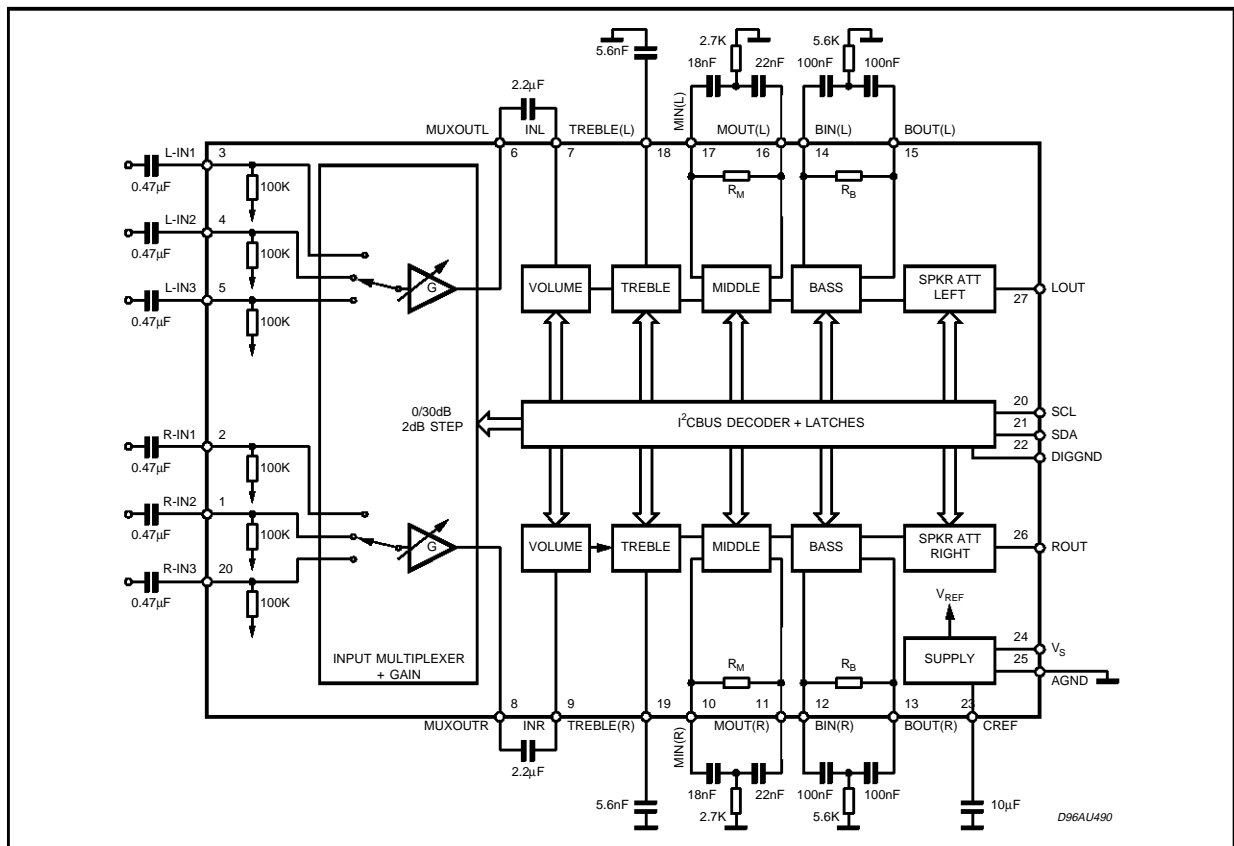
- 1) The device is functionally good at  $V_S = 5\text{V}$ . a step down, on  $V_S$ , to 4V does't reset the device.
- 2) BASS, MIDDLE and TREBLE response: The center frequency and the response quality can be chosen by the external circuitry.

# TDA7438

## ELECTRICAL CHARACTERISTICS (continued.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>AUDIO OUTPUTS</b>						
V <sub>CLIP</sub>	Clipping Level	d = 0.3%	2.1	2.6		V <sub>RMS</sub>
R <sub>L</sub>	Output Load Resistance		2			KΩ
R <sub>O</sub>	Output Impedance		10	30	50	Ω
V <sub>DC</sub>	DC Voltage Level			3.8		V
<b>GENERAL</b>						
E <sub>NO</sub>	Output Noise	All gains = 0dB; BW = 20Hz to 20KHz flat		5	15	μV
E <sub>t</sub>	Total Tracking Error	A <sub>V</sub> = 0 to -24dB		0	1	dB
		A <sub>V</sub> = -24 to -47dB		0	2	dB
S/N	Signal to Noise Ratio	All gains 0dB; V <sub>O</sub> = 1V <sub>RMS</sub> ;		106		dB
S <sub>C</sub>	Channel Separation Left/Right		80	100		dB
d	Distortion	A <sub>V</sub> = 0; V <sub>I</sub> = 1V <sub>RMS</sub> ;		0.01	0.08	%
<b>BUS INPUT</b>						
V <sub>IL</sub>	Input Low Voltage				1	V
V <sub>IH</sub>	Input High Voltage		3			V
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = 0.4V	-5		5	μA
V <sub>O</sub>	Output Voltage SDA Acknowledge	I <sub>O</sub> = 1.6mA		0.4	0.8	V

## TEST CIRCUIT



## I<sup>2</sup>C BUS INTERFACE

Data transmission from microprocessor to the TDA7438 and vice versa takes place through the 2 wires I<sup>2</sup>C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

### Data Validity

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

### Start and Stop Conditions

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

### Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an ac-

knowledge bit. The MSB is transferred first.

### Acknowledge

The master ( $\mu$ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

### Transmission without Acknowledge

Avoiding to detect the acknowledge of the audio processor, the  $\mu$ P can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

Figure 3: Data Validity on the I<sup>2</sup>C BUS

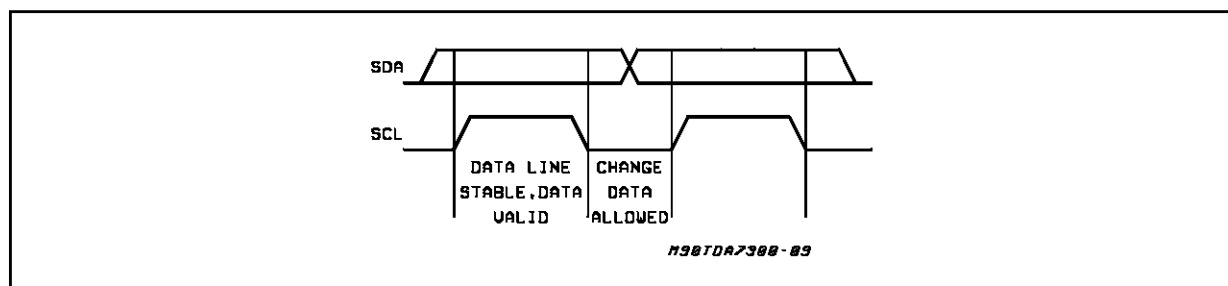


Figure 4: Timing Diagram of I<sup>2</sup>C BUS

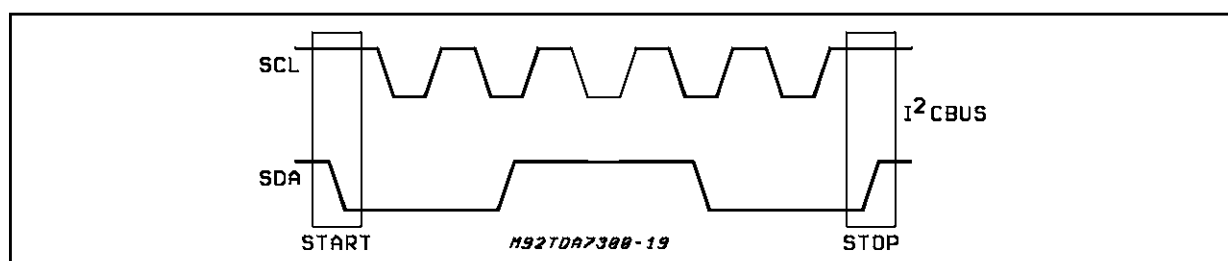
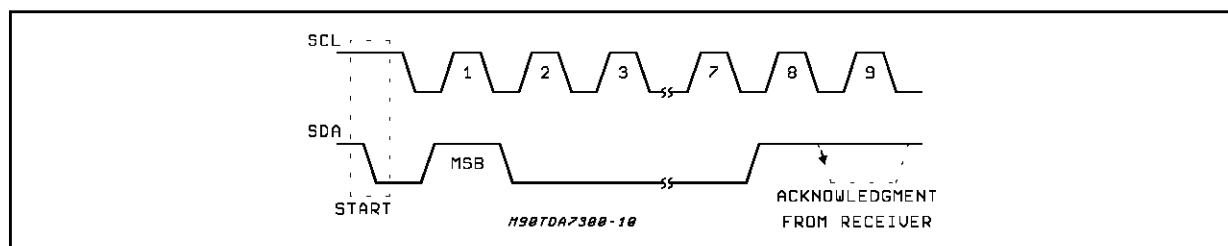


Figure 5: Acknowledge on the I<sup>2</sup>C BUS



# TDA7438

## SOFTWARE SPECIFICATION

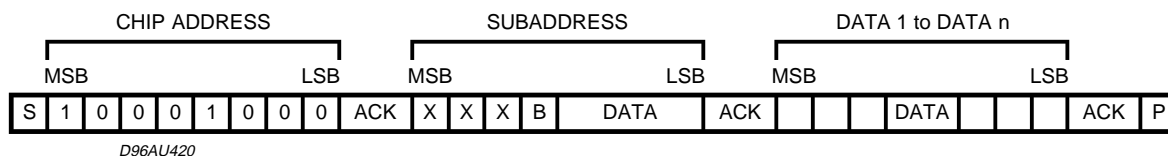
Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7438

address

- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P)



ACK = Acknowledge

S = Start

P = Stop

A = Address

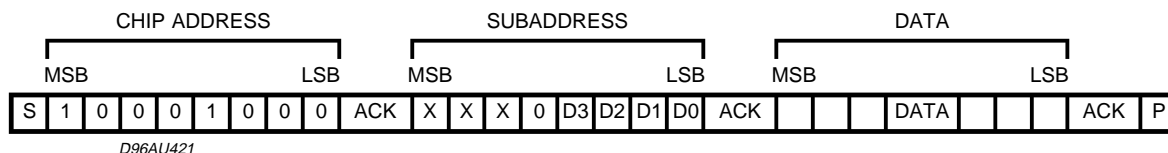
B = Auto Increment

## EXAMPLES

### No Incremental Bus

The TDA7438 receives a start condition, the cor-

rect chip address, a subaddress with the B = 0 (no incremental bus), N-data (all these data concern the subaddress selected), a stop condition.

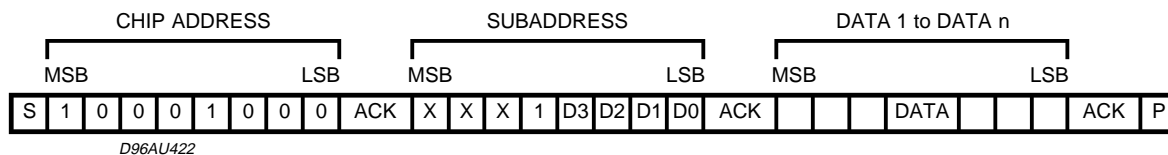


### Incremental Bus

The TDA7438 receive a start conditions, the correct chip address, a subaddress with the B = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas

SUBADDRESS from "XXX10000" to "XXX10111" of DATA are ignored.

The DATA 1 concern the subaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receives the stop condition.



## POWER ON RESET CONDITION

INPUT SELECTION	IN2
INPUT GAIN	28dB
VOLUME	MUTE
BASS	0dB
MIDDLE	2dB
TREBLE	2dB
SPEAKER	MUTE

## DATA BYTES

Address = 88 HEX (ADDR:OPEN).

FUNCTION SELECTION: First byte (subaddress)

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	B	0	0	0	0	INPUT SELECT
X	X	X	B	0	0	0	1	INPUT GAIN
X	X	X	B	0	0	1	0	VOLUME
X	X	X	B	0	0	1	1	BASS
X	X	X	B	0	1	0	0	MIDDLE
X	X	X	B	0	1	0	1	TREBLE
X	X	X	B	0	1	1	0	SPEAKER ATTENUATE "R"
X	X	X	B	0	1	1	1	SPEAKER ATTENUATE "L"

B = 1: INCREMENTAL BUS ACTIVE

B = 0: NO INCREMENTAL BUS

X = DON'T CARE

## INPUT SELECTION

MSB							LSB	INPUT MULTIPLEXER
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	X	0	0	IN3
X	X	X	X	X	X	0	1	NOT ALLOWED
X	X	X	X	X	X	1	0	IN2
X	X	X	X	X	X	1	1	IN1

## TDA7438

### DATA BYTES (continued)

#### INPUT GAIN SELECTION

MSB							LSB	INPUT GAIN
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	0dB
				0	0	0	1	2dB
				0	0	1	0	4dB
				0	0	1	1	6dB
				0	1	0	0	8dB
				0	1	0	1	10dB
				0	1	1	0	12dB
				0	1	1	1	14dB
				1	0	0	0	16dB
				1	0	0	1	18dB
				1	0	1	0	20dB
				1	0	1	1	22dB
				1	1	0	0	24dB
				1	1	0	1	26dB
				1	1	1	0	28dB
				1	1	1	1	30dB

GAIN = 0 to 30dB

#### VOLUME SELECTION

MSB							LSB	VOLUME
D7	D6	D5	D4	D3	D2	D1	D0	1dB STEPS
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	X	1	1	1	X	X	X	MUTE

VOLUME = 0 to 47dB/MUTE



**DATA BYTES (continued)****BASS SELECTION**

<b>MSB</b>							<b>LSB</b>	<b>BASS</b>
<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>2dB STEPS</b>
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

**MIDDLE SELECTION**

<b>MSB</b>							<b>LSB</b>	<b>MIDDLE</b>
<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>2dB STEPS</b>
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

## TDA7438

### DATA BYTES (continued)

#### TREBLE SELECTION

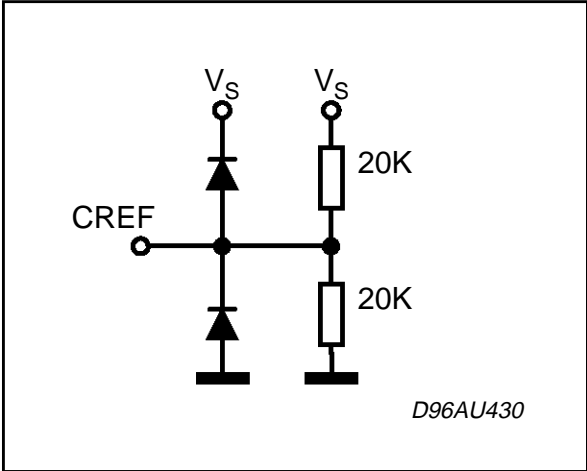
MSB							LSB	TREBLE
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

#### SPEAKER ATTENUATE SELECTION

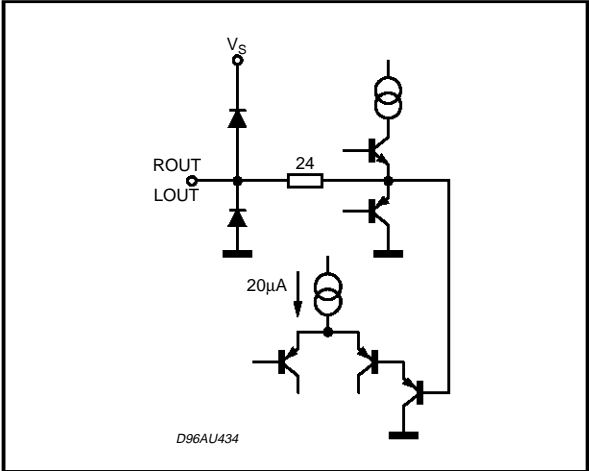
MSB							LSB	SPEAKER ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	1dB
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	0	1	1	0				-48dB
	0	1	1	1				-56dB
	1	0	0	0				-64dB
	1	0	0	1				-72dB
	1	1	1	1	X	X	X	MUTE

SPEAKER ATTENUATION = 0 to -79dB/MUTE

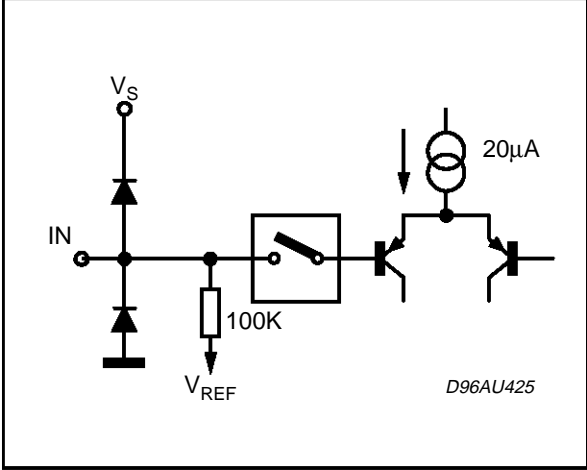
PINS: 23



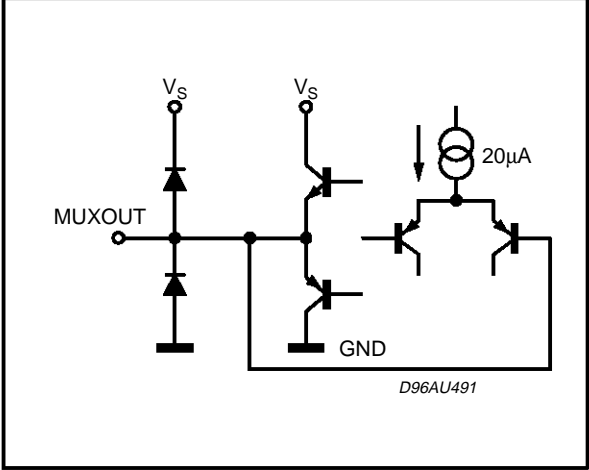
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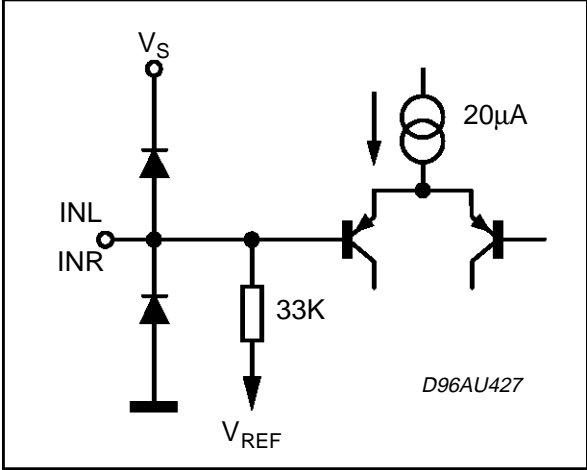
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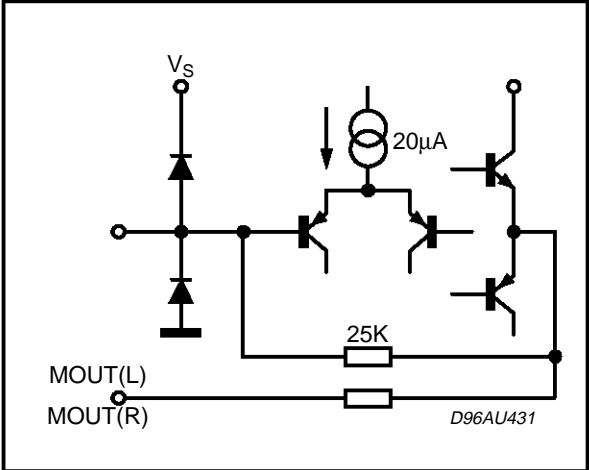
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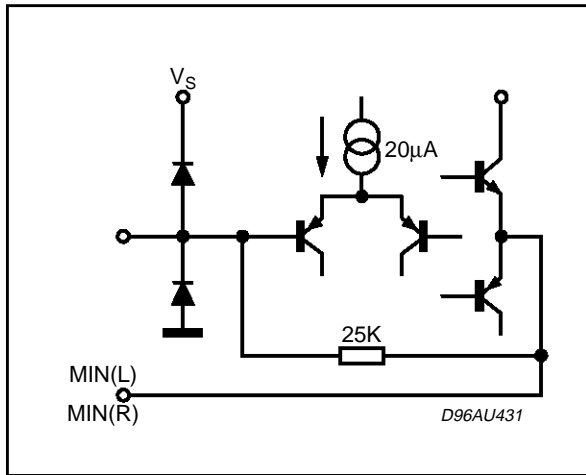
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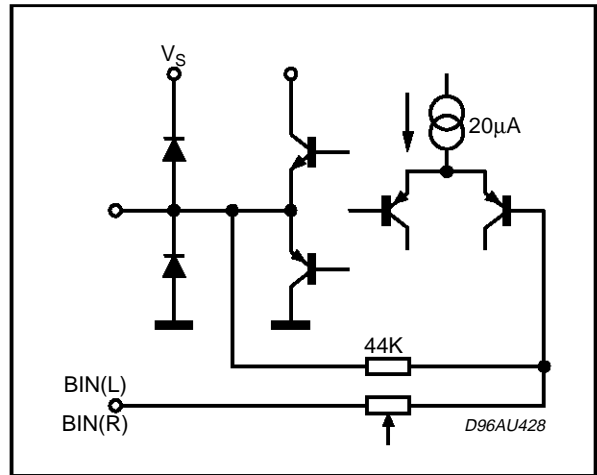
PINS: 10, 11



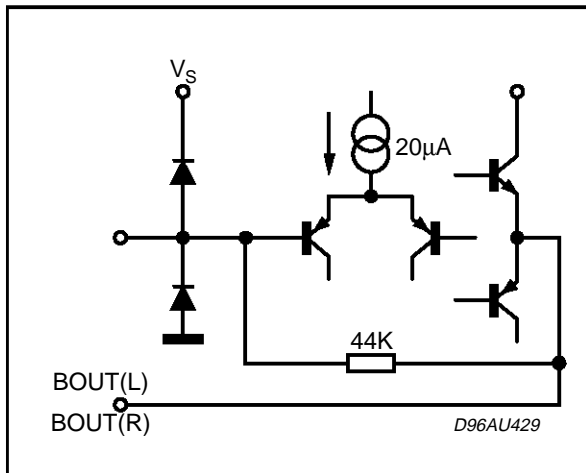
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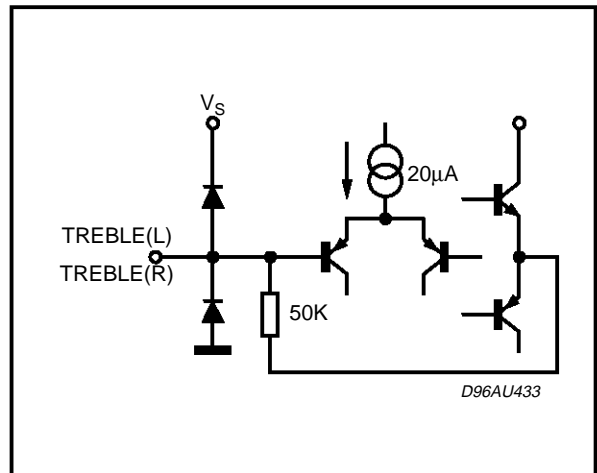
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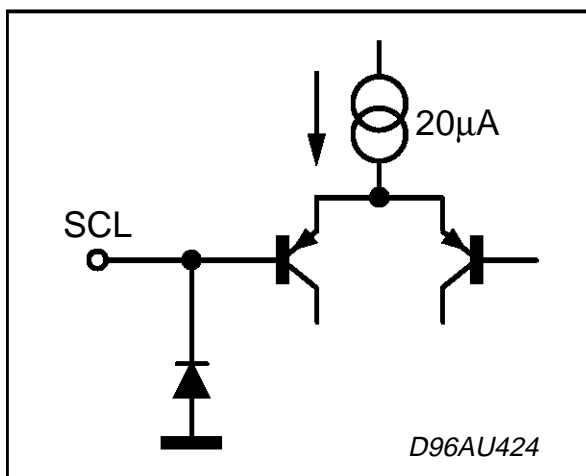
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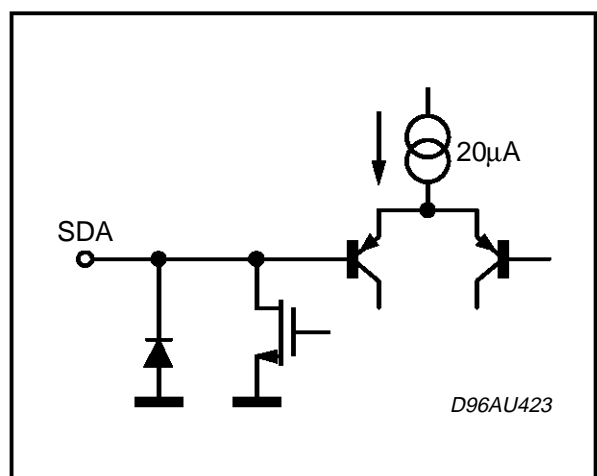
PINS: 18, 19



PINS: 20

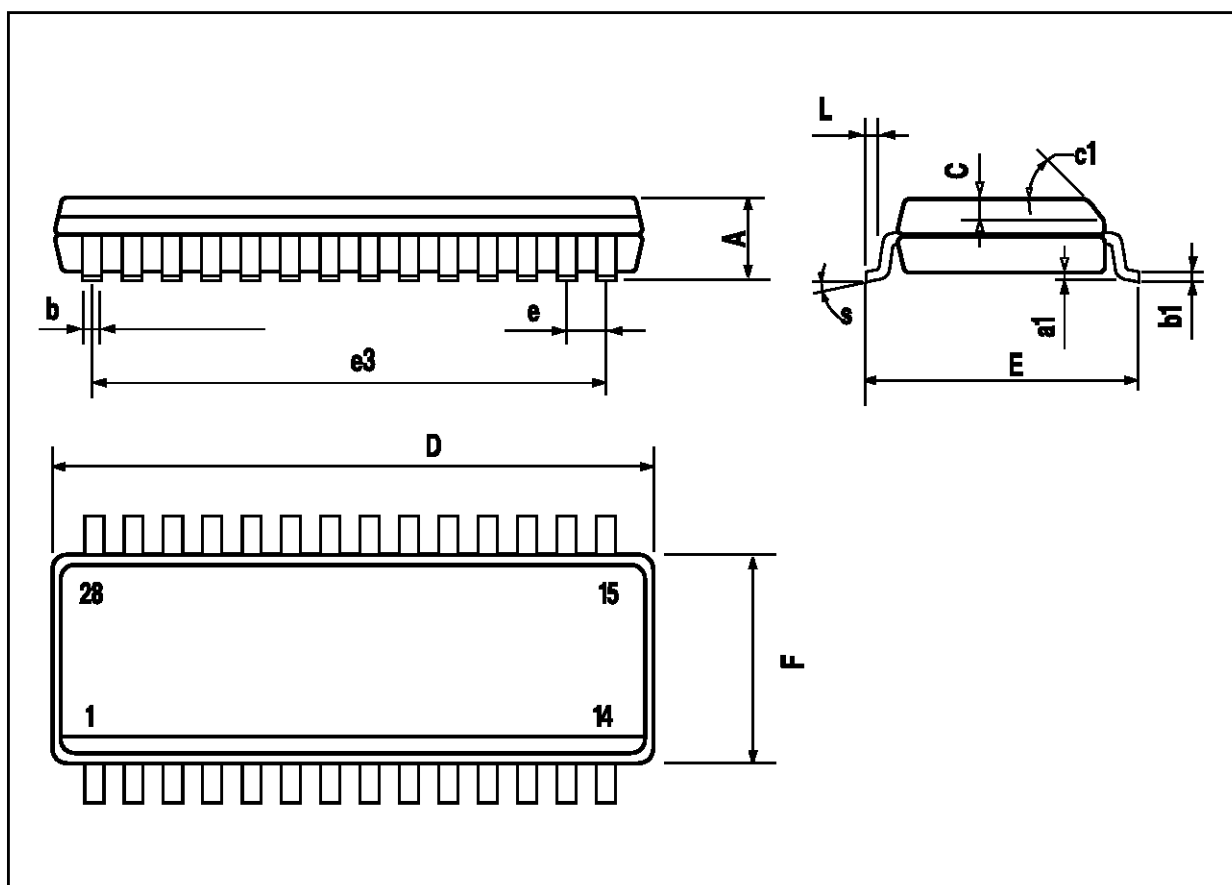


PINS: 21



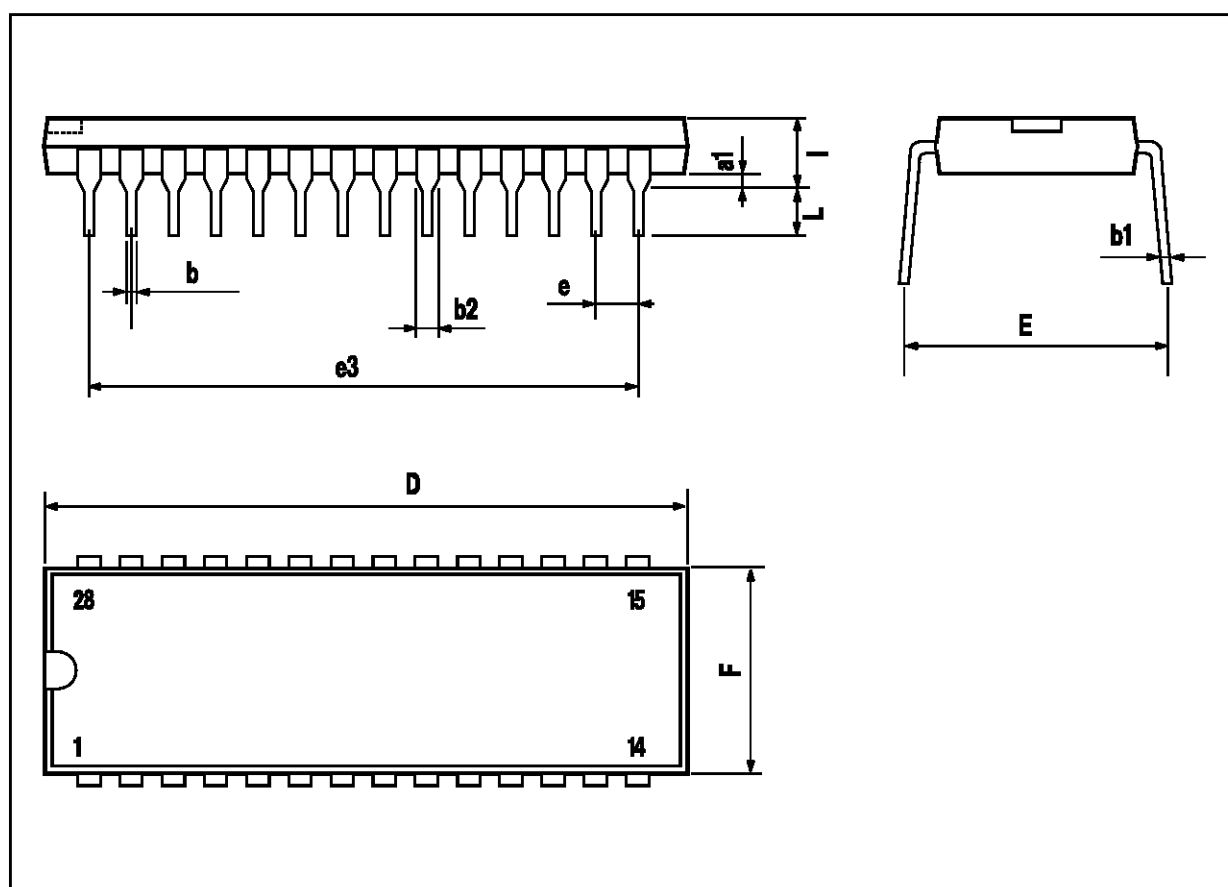
## SO28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (max.)					



# TDA7438

DIM.	mm			inch		
	MIN	TYP	MAX	MIN	TYP	MAX
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



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